AUTOMATIC GAIN CONTROL SYSTEM FOR HIGH FREQUENCY LOW IF RECEIVERS

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Abstract:

Automatic Gain Control circuits are employed in many systems where the amplitude of the incoming signal can vary over a wide range. The role of the AGC circuit is to provide relatively constant output amplitude so that circuits following the AGC circuit require less dynamic range. An Automatic gain control system intended for high frequency low IF receiver applications is designed and implemented. The specifications for the design are taken for a typical GSM 900 receiver, which usually belongs to the above class of receivers. The implemented AGC achieves 60dB dynamic range and the output settles within 75usec. The designed AGC is simulated under various process corners using Cadence tools (0.18um technology).

Keywords: Automatic Gain Controller (AGC), high frequency low IF receiver, Variable Gain Amplifier (VGA)

1.Introduction:

Automatic Gain Control (AGC) was implemented in first radios for the reason of fading propagation (defined as slow variations in the amplitude of the received signals) which required continuing adjustments in the receiver's gain in order to maintain a relative constant output signal. Automatic gain control circuits are usually employed in both the transmitter and receiver. In the receiver path, AGC is used to dynamically amplify the received signal to a stable rated strength level. In the transmitter path, because the components in this path are achieved by different chips and have signal strength levels, the role of the AGC circuits are to provide a relatively constant output amplitude.

1.1. Objectives:

The main objective is both analysis and design of an Automatic Gain Control[1],[2], circuit for wireless communication systems, especially suitable for the GSM receiver application.

1.2. Schematic Diagram:

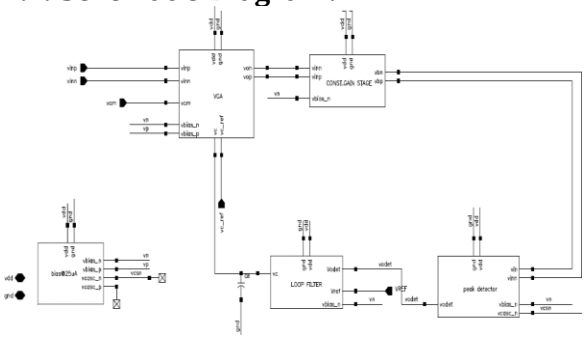


Figure.1: Block level schematic of the implemented AGC

2. Problem Characterization:

In GSM 900 standard, the received signal at the cellular base station varies typically from -102dBm to -12dBm. This large variation in the received signal power may saturate some of the receiver blocks. The need for signal dynamic range compression arises here. Also, this compression must be linear and it should not saturate the output as in a limiter. Considering this, an automatic gain control amplifier[2] is used to reduce the signal dynamic range linearly and to provide relatively constant signal level to the circuits following.

2.1. System level specifications:

Generally, a low IF architecture is chosen for highly integrated narrowband receivers to minimize the system cost and power consumption. Here, the chosen IF is 5MHz. So, the AGC must process 5MHz signal. The signal power level at the AGC input varies from -15dBm to -85dBm. Without the interferer, the minimum power level required at the ADC input is typically -8dBm. Considering this, the minimum output power level of AGC is set to -5dBm. The output power level of AGC varies from +5dBm to -5dBm. From this distribution it is clear that AGC must provide 60dB dynamic range to the IF signal before it is processed by ADC.

2.2. Block level specifications:

From the system specification it is clear that AGC forward path must have gain range of 20- 60dB. In this design the AGC forward path composed of VGA followed by a fixed gain amplifier. The Variable Gain Amplifier is required to provide a gain variation of 0-

60dB. The constant gain stage provides 20dB gain to boost the signal to the desired level.

The design equations for the AGC loop parameters with specified settling time and Q factor are given by

Forward Path Gain (K) = $\alpha . V_{out}. Ag$

Low Pass Filter Pole (Pl) = Wn. Q

Integrator Unity Gain Frequency (fu) = $Wn^2/Ad. Pl. K$

Block	Parameter	Value
VGA	Gain Range	0-60dB
	Bandwidth	>70MHz
	Noise Figure	15dB
	1dB compression point	-16dBm
Constant Gain Stage	Gain	20dB
	Bandwidth	>200GHz
Loop Filter	Unity Gain Frequency	34kHz

Table.1: Specifications of the individual blocks

3. AGC system design:

3.1 Introduction:

The main blocks in AGC loop are VGA block, Constant Gain stage, Peak Detector and Loop Filter.

3.2 VGA Block:

The desired gain range of 0-60dB is distributed among four identical Variable Gain Amplifier stages. The Gain range of each VGA is 0-15dB. The bandwidth of each stage VGA is decided considering the reduction in bandwidth when identical stages are cascaded. Consider an amplifier chain consisting of N identical stages each with a gain of Av and bandwidth of fs. The below Equation gives the relation between the bandwidth of each stage and the whole amplifier chain

$$fs = \frac{ft}{\sqrt{2^{\frac{1}{N}} - 1}}$$

Where ft is the bandwidth of the overall amplifier chain.

The schematic of gain cell along with the common mode feedback circuit is shown in Fig 3. The gain cell composed of source coupled pair with diode connected loads. The currents through input pair and load are constant that are equal to the upper P-MOS current sources.

The gain control mechanism can be achieved by mirroring the gain control block differential output currents (Ib and Ia) to the tail currents of input source coupled pair and load respectively. Current mirrors are long channel devices for better mirroring precision.

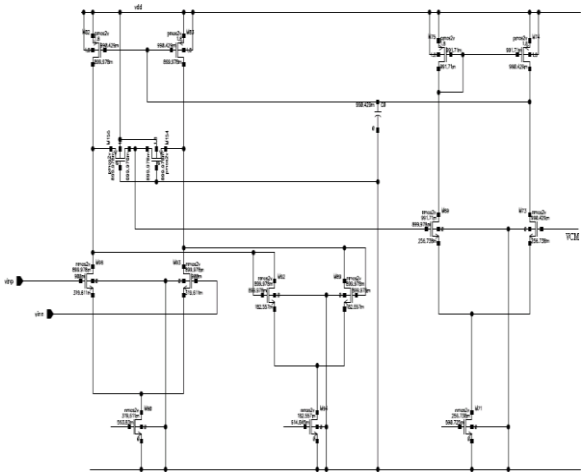


Figure.2: Circuit implementation of the variable gain block.

If the square law is applied and all the bulk of NMOS devices are tied together, differential gain that is determined by the input and load transconductance ratio can be expressed as:

$$Gain = \frac{g_{minput}}{g_{mload}}$$

$$= \sqrt{\frac{\mu_n C_{ox}(W/L)iI_i}{\mu_n C_{ox}(W/L)_l I_l}}$$

$$= \sqrt{\frac{\mu nCox(W/L)i(I_{BIAS} + I_{CONT})}{\mu nCox(W/L)l(I_{BIAS} - I_{CONT})}}$$

$$= K\left(\frac{1+x}{1-x}\right)^{\frac{1}{2}}$$

By cascading the two identical gain cells, the desired dynamic gain control range 30dB is achievable. It can be seen in Fig.2, the gain control range is from -15dB to 15dB. In our AGC system, however, the useful gain range has to be positive. To shift the gain curve up, the variable K that is determined by device size ratio should be set appropriately. The bandwidth of the Variable Gain Amplifier is determined by the output impedance and capacitance. Compared with the Gilbert cell that may have a constant bandwidth for different gain setting, the bandwidth of the proposed VGA cell has a little difference because the output impedance (1/gm) varies with the square root of the control current.

The Common Mode Feedback (CMFB) is required in order to prevent any of the transistors from entering from linear mode of operation and to maintain a specific DC value for the biasing of the next stage. In this design, the CMFB consists of a simple resistive divider and an error amplifier. The resistive divider,

implemented with PMOS operating in triode region, senses the common mode voltage.

The error amplifier compares this value with the desired common mode value and amplifies the error voltage. The error difference controls the gate voltage of current sources in VGA in such a way that the output common mode remains at the desired value. The CMFB loop is compensated by placing a large capacitance at the output of the error amplifier.

3.3. Constant Gain Stage:

Normally the constant gain stage is used in the forward path to boost the signal to the desired level. However, in this application it must also have good linearity performance. Cascaded VGA may not fulfill the linearity requirement. Since the more complexity architecture of VGA, the linearity would be degraded compared to with a simple constant gain differential amplifier. Since the linearity is dominated by the last stage of cascade amplifiers, good linearity amplifier should be put at the last stage.

Although the reduction complexity for simple differential amplifier already minimizes parasitic capacitance, the miller effect exists and significantly reduces the overall frequency response. There are some techniques like negative resistive load to enhance the frequency response, but the drawback of voltage headroom and not suitable for low voltage supply. Therefore, neutralization technique is a good candidate for low power and low voltage supply in order to eliminate the miller effect.

Without including the capacitance C_{GDN}, the capacitance seen at the gate of the transistor M1 is given by

$$C_{in} = C_{GS1} + C_{GD1}(1-Av)$$

where Av is the gain from the gate to the drain of M1. Since the amplifier is perfectly balanced, the gain from the gate of M1 to the drain of M2 is -Av. As a result, the total capacitance at the gate of M1 after including capacitor C_{GDN} in the circuit is given by

$$C_{in} = C_{GD1}+C_{GS1}(1-Av) + C_{GDN1}(1+Av)$$

If the value of C_{GDN} is selected such that $C_{GDN} = C_{GD1}$, above equation simplifies to

$$C_{in} = C_{GS1}+2C_{GD1}$$

This is very similar to the input capacitance of a cascode configuration.

Capacitors C_{GDN} are implemented as transistors M_{21} and M_{22} as shown in Fig.3. Since M1 and M2 are in the saturation region,

$$V_{DS}(M1,M2) \geq V_{GS}(M1,M2) - V_{T1}$$

$$\Rightarrow V_{GD}(M1,M2) \leq V_{T1}$$

$$V_{GS}(M12,M22) \leq V_{T1}$$

Hence, transistors M_{21} and M_{22} operate in the cut-off region, with C_{GDN} being equal to the sum of their gate-to-drain and gate-to-source overlap capacitances.

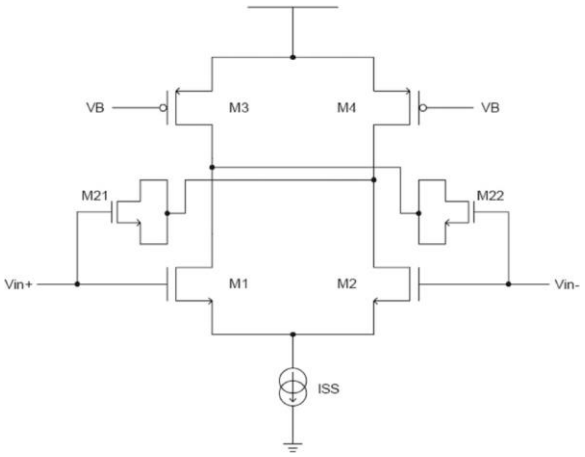


Figure.3: Capacitive neutralization with MOS transistors as capacitors

3.4. Peak Detector:

In the AGC feedback loop, the peak detector[3] (envelop detector) is used to monitor the strength of the signal by detecting the peak value of the signal

Circuit Implementation:

The designed differential peak detector circuit is shown in the below Figure.5.

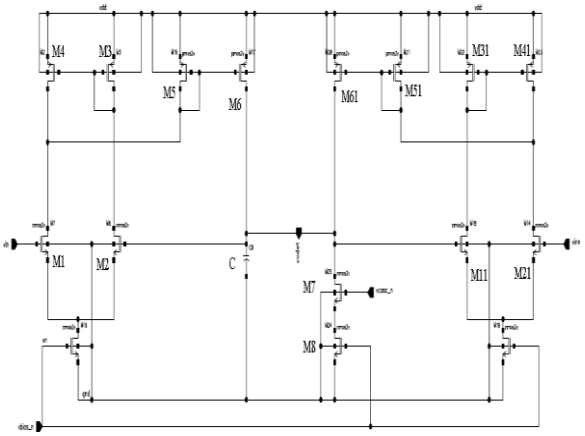


Figure.4. Implementation of Differential peak detector

In this design, diode is replaced with a current mirror M5 an M6.

3.5. Integrator:

Integrator along the feedback path of Automatic gain control performs three functions. It compares the detectors output with the reference voltage, smooths this difference signals, then sends back to control the VGA gain. In order to perform these three functions, the integrator is realized in transconductor (gm) – capacitor (C) topology.

the unity gain frequency is: $ft = \frac{g_{mM2}}{2\pi C}$

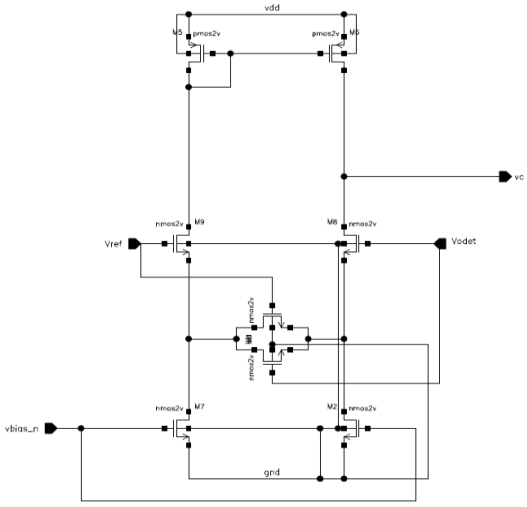


Figure.5: Implementation of OTA-C integrator with source degeneration

the integrator is designed for a nominal gain of 40dB and for UGF of 27 kHz. To obtain the required low UGF an external capacitor of 1nF is used (not shown in Figure).

3.6. Bias Circuit:

The bias circuit used in the design is a wide swing constant transconductance[6] bias circuit as shown in Fig.7. The wide swing current mirror greatly minimizes most of the detrimental second order imperfections caused by the finite output impedance of the transistors, without greatly restricting signal swings. Using this type of bias circuit provides wide signal swing for the gain cell by reducing the overdrive required for the bias transistors.

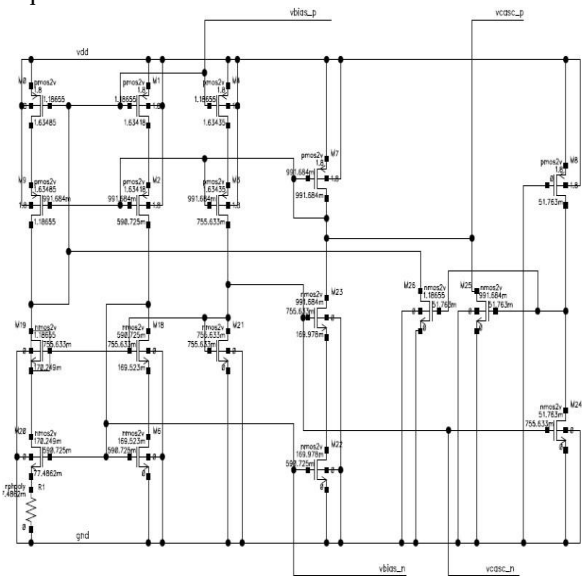


Figure.6: Wide swing constant-transconductance bias circuit

The bias circuit is designed for a current of I_{BIAS} =25uA. A start-up circuit is also designed to avoid the condition of zero current in all transistors at the start-up. The bias current varies less than 25% for typical-typical process corner.

4. Simulation Results:

4.1. Variable Gain Amplifier:

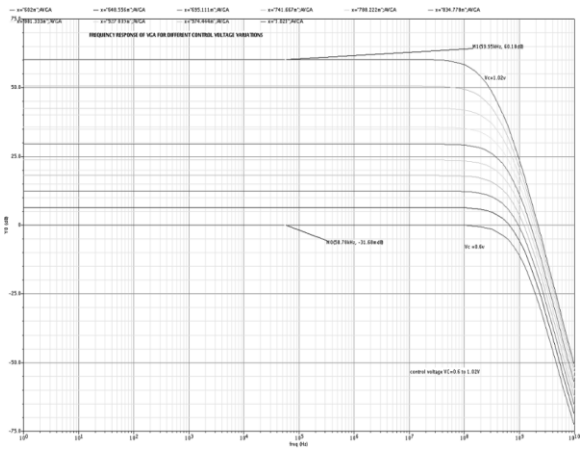


Figure.7: Frequency Response of VGA for various control voltages

The gain of overall VGA block varies from 0db to 60dB for a gain control voltage range of 0.6v to 1.02v. The bandwidth varies slightly from 145MHz to 400MHz.

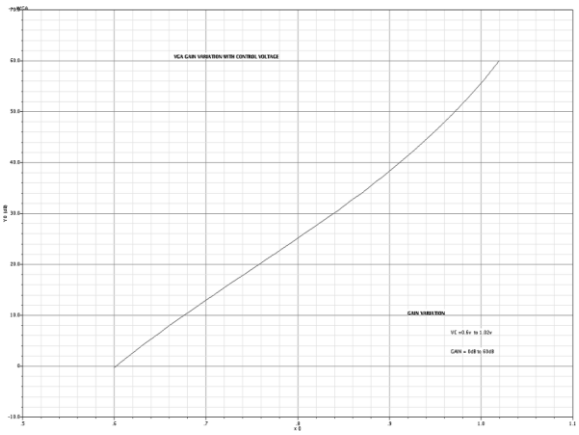


Figure.8: dB-linear variation of VGA gain with respect to control voltage

The VGA gain characteristic shows a gain variation of 3dB from its mean value at the low gain end. However, at high gain end the variation is less than 1dB from mean value.

From the simulation result, it is clear that the designed VGA possesses dB- linear characteristics i.e. the gain expressed in decibels varies linearly with the control voltage. Here the gain varies from 0-60dB for a control range of 0.6-1.02v. The deviation from the ideal logarithmic curve is less than ±0.5dB.

4.2. Constant Gain stage:

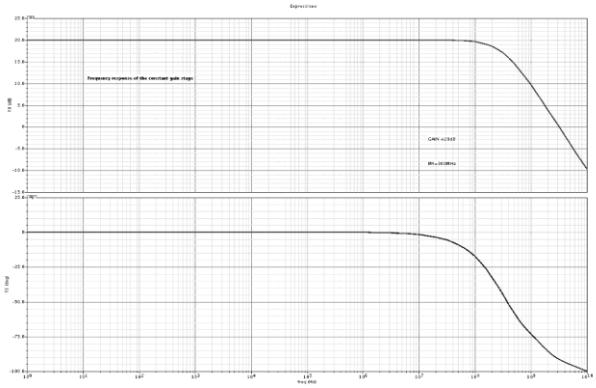


Figure.9: Frequency response of the Constant Gain Stage.

The constant gain stage provides a constant 20dB gain for frequencies up to 300MHz.

4.3. AGC forward path:

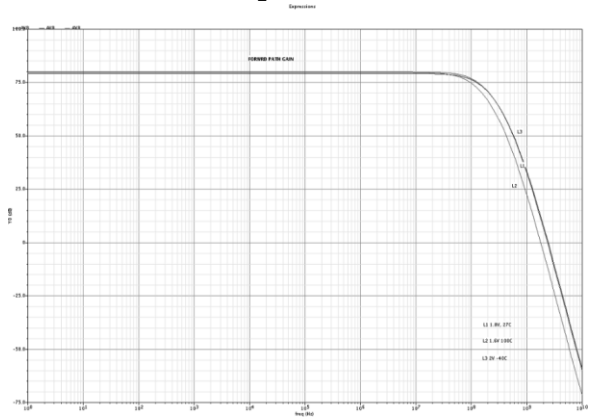
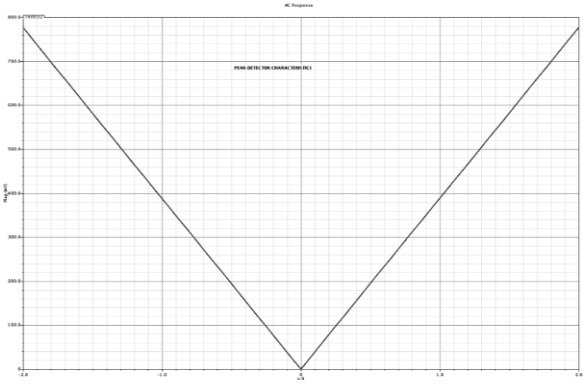


Figure.10: Frequency response of AGC forward path @ different corners

The measured value of Noise Figure is 3.22dB measured at the maximum gain setting. The measured value of the 1dB compression point for the forward path is -14dBm.From the theoretical point of view, the IIP3 is 10dB above this point. So, the IIP3 for the forward path is -4dBm measured at the minimum gain (i.e. at maximum input signal level).

4.4. Peak Detector:



Figur.11: Peak Detector Characteristics (input signal amplitude Vs output)

4.5. Loop Filter:

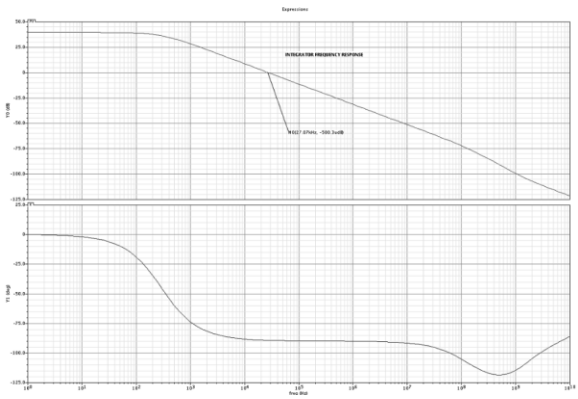


Figure.12: Integrator Frequency Response

4.6. AGC System:

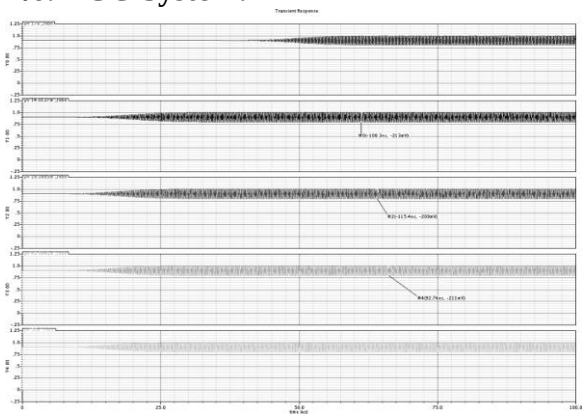


Figure.13: AGC output settling times for different input signal levels

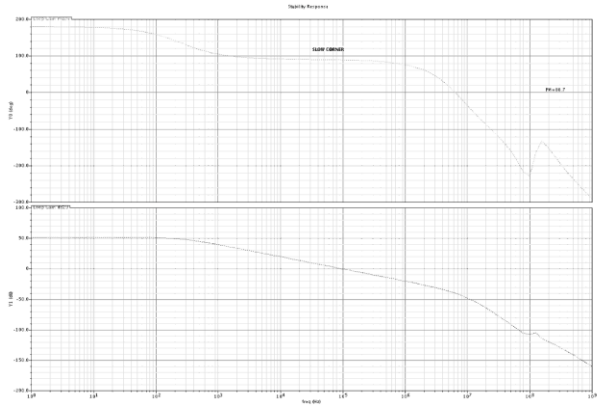


Figure.14: Closed loop frequency response of AGC at Slow corner (1.6v, 120˚C)

5. Future Scope and Conclusion:

The conventional feedback type AGC is designed and implemented for GSM receiver IF application. The designed AGC met all the specifications required for it to be employed in a typical GSM receiver. The simulation result confirms the db-linear characteristics of VGA to an acceptable level. The settling time requirement was met and it is below the required value of 100u seconds. As required by the system, the settling time is not too low or not too high but comparable to

the specification value. A too small value here makes the AGC loop to respond to unnecessary noise variations. So, the obtained settling time is satisfactory.

However, the implemented AGC can be considered as a linear system only under certain small signal approximation that the output amplitude of AGC is operating under its fully converged state. This is due to the omission of the logarithmic amplifier in the AGC feedback loop. The loop can be made perfectly linear by including the logarithmic amplifier just before the comparator block. Then the loop characteristics will be independent of any type of "bias" values including Vref.

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